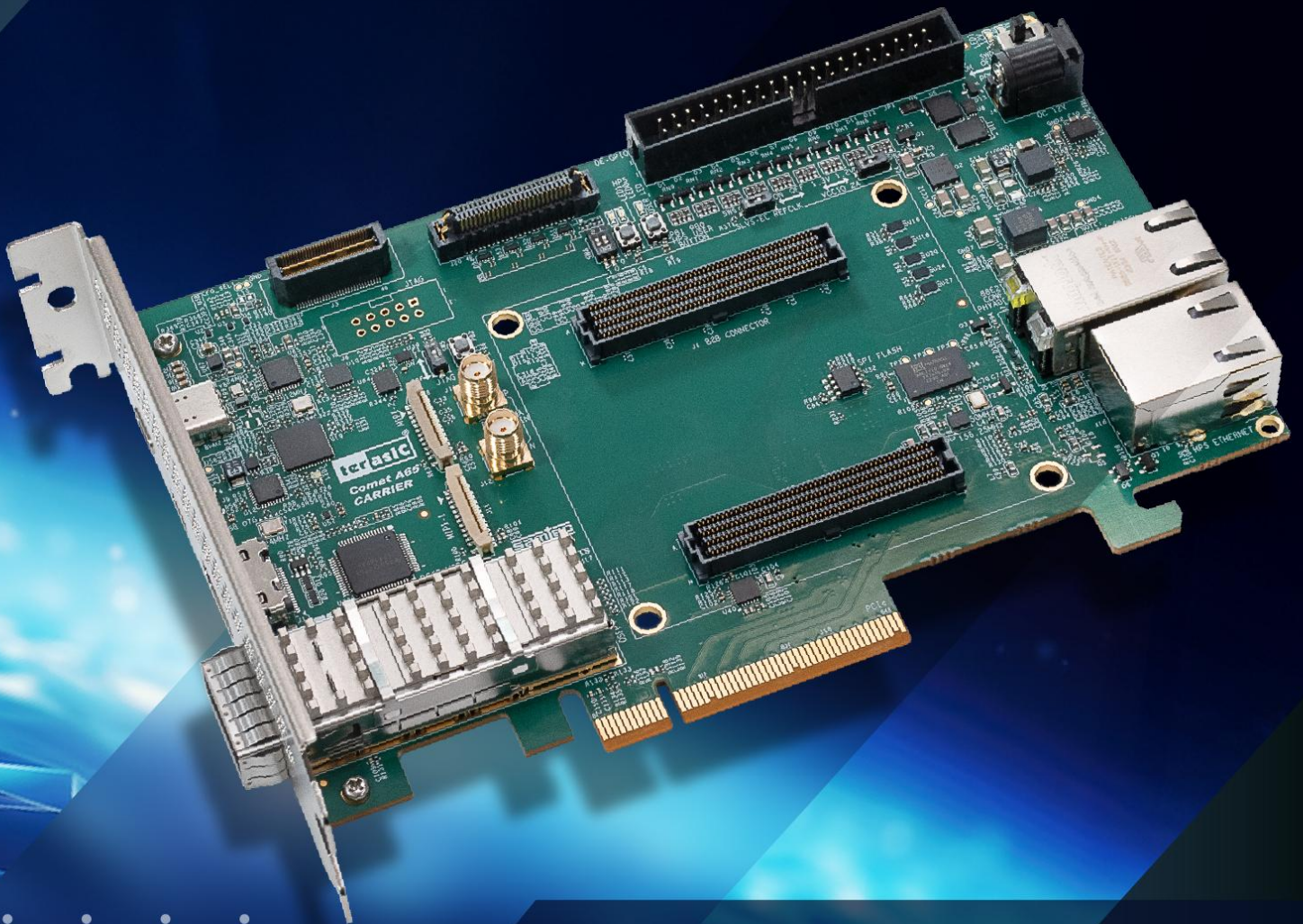


Comet-A65 Carrier Board



Design Guide

CHAPTER 1	<i>ABOUT THIS GUIDE</i>	3
CHAPTER 2	<i>POWER AND RESET</i>	4
2.1	GENERAL POWER REQUIREMENTS	4
2.2	POWER-UP SEQUENCE	4
2.3	POWER ENABLE SIGNALS	5
2.4	POWER STATUS SIGNALS	5
CHAPTER 3	<i>COMET A65 BOARD INTERFACE</i>	7
3.1	MODULE CONNECTORS	7
3.2	TRANSCEIVERS	7
3.3	JTAG INTERFACE	8
3.4	LVDS PIN PLACEMENT RESTRICTIONS	8
3.5	HPS I/O PIN ASSIGNMENTS	11
3.6	RESET SIGNALS	12
3.7	BOOT CONFIGURATION SIGNALS	12
3.8	TRACE-LENGTH MATCHING BETWEEN SOM AND CARRIER BOARDS	13
CHAPTER 4	<i>MECHANICAL AND HEATSINK DESIGN</i>	14
4.1	INTRODUCTION	14
4.2	HEATSINK	14
4.3	MECHANICAL DIMENSIONS	14
CHAPTER 5	<i>ASSEMBLY & DISASSEMBLY</i>	20
5.1	ASSEMBLY & DISASSEMBLY FOR SOM AND CARRIER	20
5.2	3D CAD FILES	20
CHAPTER 6	<i>POWER CONSUMPTION MEASUREMENT</i>	21
6.1	POWER MONITORING SYSTEM	21
	<i>ADDITIONAL INFORMATION</i>	22

Chapter 1

About this Guide

This document provides guidelines for designing a custom carrier board compatible with the Comet A65 Agilex 5 SoC SOM. It includes information on power-up sequencing, control signal management, JTAG connection, EEPROM programming, HPS I/O constraints, and connector pin assignments.

Chapter 2

Power and Reset

2.1 General Power Requirements

The carrier board must provide the following power rails :

Table 1-1 Part Number of the connector on the Titan S10 SOM

Pin Name	Description	Voltage
VIN	Power input to the SOM.	5V ~ 12V
VCCIO_xx	<p>FPGA VCCIO rails supplied at voltage levels appropriate for the FPGA I/O standards in use.</p> <p>These FPGA VCCIO rails should be enabled by GROUP3_PWR_EN signal, the soft-start time of these FPGA VCCIO rails should between 1 msec and 3 msec.</p>	User Defined
VCC12_FAN	Power input for the SOM cooling fan.	12V

2.2 Power-Up Sequence

The power-up sequence is critical. The carrier board must respect the ramp times (1 to 3 msec for FPGA VCCIO rails)

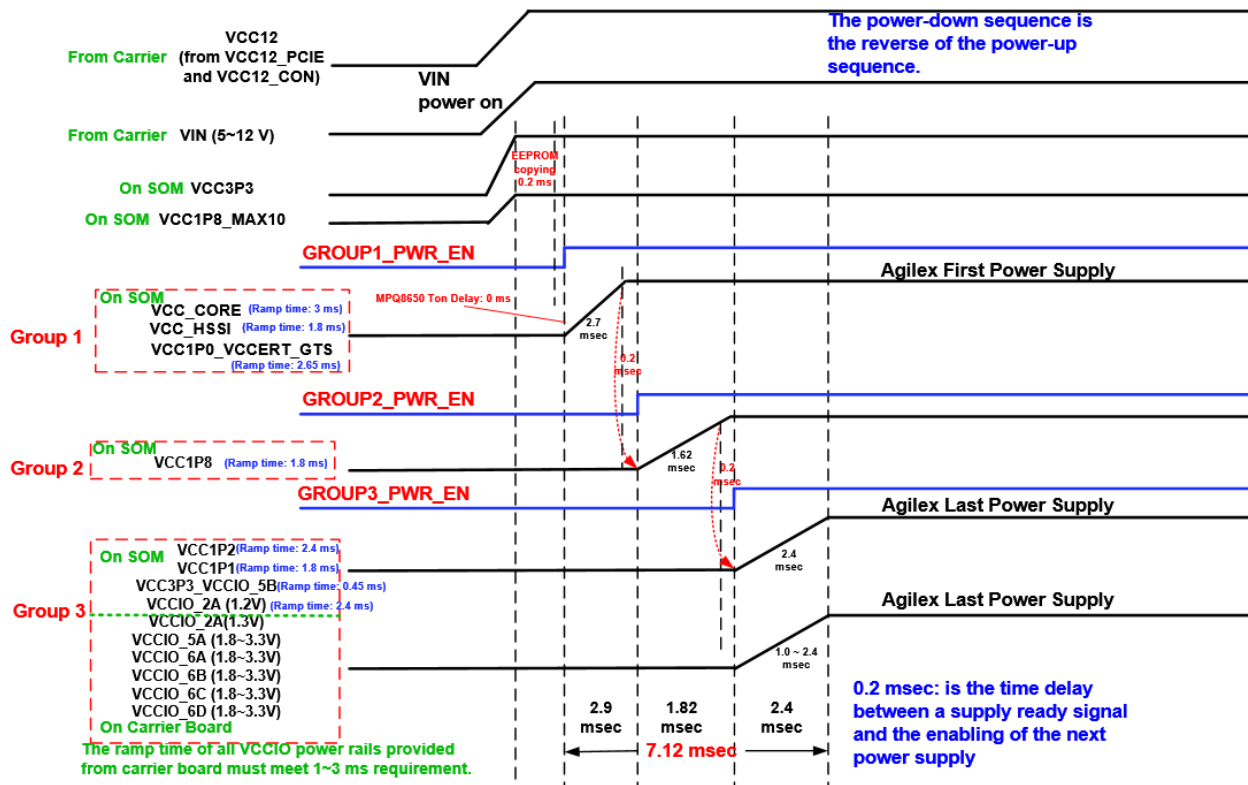


Figure 2-1 Power Up Sequence for Comet A65 SOM and Carrier Board

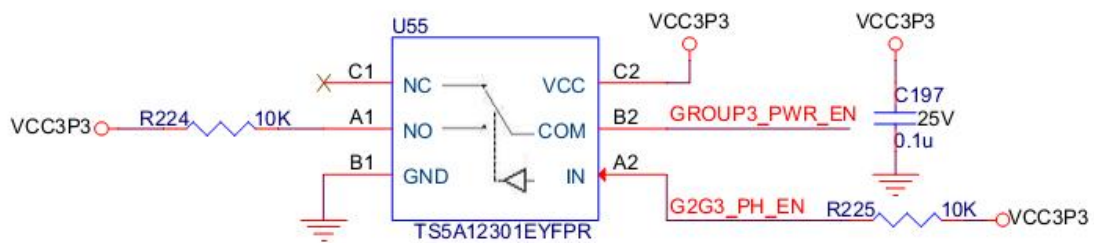
2.3 Power Enable Signals

- **GROUP2_PWR_EN**: Enables the 1.8V power supply for HPS peripheral devices on the carrier board.
- **GROUP3_PWR_EN**: Enables the FPGA VCCIO power rails on the carrier board.
- **VCCIO_2A_1V2_EN**: Configures the VCCIO power for FPGA sub-bank 2A to either 1.2V or 1.3V. 1.2V is default setting.
 - ◆ Logic High: VCCIO_2A of the FPGA is set to 1.2V, supplied by the SOM.
 - ◆ Logic Low: VCCIO_2A of the FPGA is set to 1.3V, supplied by the carrier.

2.4 Power Status Signals

- **VCCIO_XX_PG**: Power-good signals asserted when corresponding FPGA VCCIO rails on the carrier board are operating normally. These signals inform the SOM that carrier-provided corresponding VCCIO power rails are ready.

- **G2G3_PH_EN:** Detection signal used to identify SOM insertion.
 - ◆ Should be connected to J2 pin-D49. The J2 pin-D49 on SOM is connected to GND. This G2G3_PH_EN signal must be pulled high on the carrier board.
 - ◆ When the G2G3_PH_EN signal is pulled high, GROUP2_PWR_EN and GROUP3_PWR_EN are also pulled high, allowing the carrier power rails to be enabled even without the SOM installed.
 - ◆ This enables verification of all carrier power rails before SOM insertion.
 - ◆ The following is the design example for G2G3_PH_EN :



IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L or Open	ON	OFF
H	OFF	ON

When G2G3_PH_EN is pulled high, GROUP2_PWR_EN and GROUP3_PWR_EN are also pulled high, enabling verification of carrier rails even without the SOM installed

Comet A65 Board Interface

3.1 Module Connectors

The Comet A65 SOM connects to the carrier board via high-density **B2B** connectors.

- **Carrier Board Connector:** Samtec SEAF8, 400-pin female connector (P/N: SEAF8-50-05.0-S-08-3)
- **SOM Connector:** Samtec SEAM8, 400-pin male connector (P/N: SEAM8-50-S02.0-S-08-3)

With the recommended connectors, the stack height between the Comet A65 SOM and the carrier board is **7 mm**.

For detailed pinout assignments of the B2B connectors (J1 and J2), please refer to the pinout tables provided in the engineering documentation: [Comet_A65_Pinout.xlsx](#).

3.2 Transceivers

Connectors J1 and J2 each provide two pairs of transceiver reference clock pins, allowing the carrier board to supply the necessary clock signals to the FPGA transceivers.

Design and Layout Guidelines:

- **Placement Rules:** For detailed information on transceiver channel placement rules and design requirements, please refer to Chapter 2.2 of the [GTS Transceiver PHY User Guide](#).
- **Unused Pin Termination:**
 - a) **Reference Clocks:** If the provided reference clock pins on J1 and J2 are not used in the application, they must be tied to **ground** (GND).
 - b) **Input Pins:** Any unused transceiver input pins must also be terminated by connecting them to **ground**.

3.3 JTAG Interface

To enable FPGA configuration, the four JTAG signals must be connected to either a standard 2x5 JTAG pin header or an on-board USB Blaster interface.

- **IO Standard:** Please note that the FPGA JTAG interface operates at 1.8V.
- **Reference Design:** A design example for the 10-pin JTAG header implementation is shown below.

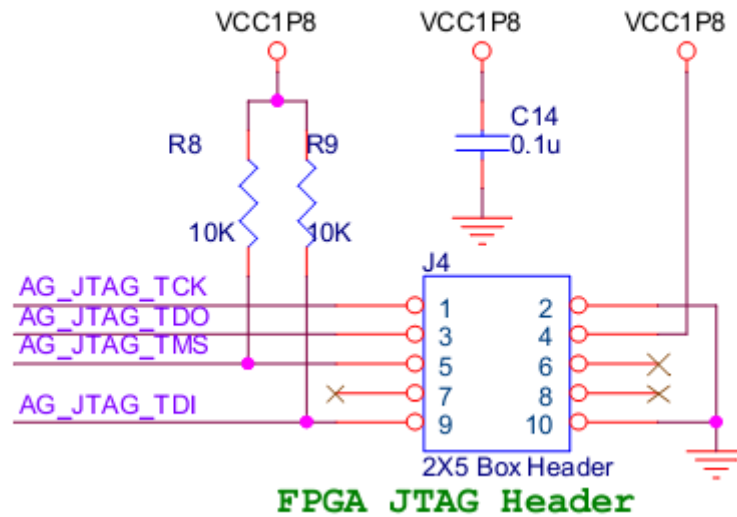


Figure 3-1 USB Blaster III shown in PC Device Manager

3.4 LVDS Pin Placement Restrictions

This section informs users that certain HSIO 2A, 2B, and 3B I/Os of the FPGA on the J1 and J2 connectors cannot be configured as LVDS signals. Please take note of these restrictions when designing the carrier board. The restricted nets are listed in the table below.

Table 3-1 Restricted HSIO 2A, 2B, and 3B Nets on J1/J2 Connectors (LVDS Unavailable)

FPGA Bank	Restricted Carrier Board Net Names
2B	J2_HSIO_2BT_A_p16 / n16
	J2_HSIO_2BT_A_p13 / n13
2A	J1_HSIO_2AT_A_p4 / n4
3B	J2_HSIO_3BT_A_p16 / n16

The detailed reasons for these restrictions are described below:

- **Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in the 2B and 3B HSIO Banks**

According to Altera Agilex 5 General-Purpose I/O User Guide, there are Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in the Same HSIO Bank. As shown in the figure below, If the user's application makes use of the LPDDR4C port, since 2B bank index 74/78 is assigned to LPDDR4 for single-ended use, the two pairs at 2B index 64/65 and 70/71 cannot be used for LVDS. Correspondingly in the carrier board schematic, the pairs J2_HSIO_2BT_A_p16 / J2_HSIO_2BT_A_n16 and J2_HSIO_2BT_A_p13 / J2_HSIO_2BT_A_n13 cannot be assigned as LVDS signals.

In a similar situation, If the user's application makes use of the LPDDR4D port, since 3B bank index 74/78 is assigned to LPDDR4 for single-ended use, the two pairs at 3B index 64/65 and 70/71 cannot be used for LVDS. Correspondingly in the carrier board schematic, the pairs J2_HSIO_3BT_A_p16 / J2_HSIO_3BT_A_n16 and J2_HSIO_3BT_A_p13 / J2_HSIO_3BT_A_n13 cannot be assigned as LVDS signals.

Table 19. Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in the Same HSIO Bank

This table lists the combinations of pins and I/O standards not allowed in the same HSIO bank. Examples:

- If you place a true differential I/O standard in pin pair 10 and 11, do not place single-ended I/O standards in pins 8 or 19.
- If you place a single-ended I/O standard in pin 57 or 67, do not place a true differential I/O standard in pin pair 58 and 59.

Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)	
True Differential Pin Pair	Single- Ended Pin	True Differential Pin Pair	Single- Ended Pin	True Differential Pin Pair	Single- Ended Pin	True Differential Pin Pair	Single- Ended Pin
0 and 1	3, 4	24 and 25	27, 28	48 and 49	51, 52	72 and 73	75, 76
2 and 3	0	26 and 27	16, 24	50 and 51	40, 48	74 and 75	64, 72
4 and 5	1, 15	28 and 29	25, 39	52 and 53	49, 63	76 and 77	73, 87
6 and 7	9	30 and 31	22, 32	54 and 55	46, 56	78 and 79	70, 80
8 and 9	6, 11	32 and 33	31, 34	56 and 57	55, 58	80 and 81	79, 82
10 and 11	8, 19	34 and 35	33, 43	58 and 59	57, 67	82 and 83	81, 90
12 and 13	14, 17	36 and 37	38, 41	60 and 61	62, 65	84 and 85	86, 89
14 and 15	5, 12	38 and 39	29, 36	62 and 63	53, 60	86 and 87	77, 84
16 and 17	13, 26	40 and 41	37, 50	64 and 65	61, 74	88 and 89	85
18 and 19	10, 21	42 and 43	35, 45	66 and 67	59, 69	90 and 91	83, 92
20 and 21	18, 23	44 and 45	42, 47	68 and 69	66, 71	92 and 93	91, 94
22 and 23	20, 30	46 and 47	44, 54	70 and 71	68, 78	94 and 95	93

Figure 3-2 USB Blaster III shown in PC Device Manager

● Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in Adjacent HSIO 2A and 2B Banks

According to Altera Agilex 5 General-Purpose I/O User Guide, there are Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in Adjacent HSIO Banks. As shown in the figure below, If the user's application makes use of the LPDDR4C port, since 2B bank index 2 is assigned to LPDDR4 for single-ended use, the pair at 2A index 88/89 cannot be used for LVDS. Correspondingly in the carrier board schematic, the pair J1_HSIO_2AT_A_p4 / J1_HSIO_2AT_A_n4 cannot be assigned as LVDS signals.

Table 20. Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in Adjacent HSIO Banks

This table lists the combinations of pins and I/O standards not allowed in adjacent HSIO banks. Examples:

- If you place a true differential I/O standard in pin pair 6 and 7 of bank 3B, do not place single-ended I/O standards in pin 95 of bank 3A.
- If you place a single-ended I/O standard in pin 2 of bank 2B, do not place a true differential I/O standard in pin pair 88 and 89 of bank 2A.

Combinations Not Allowed (Pin Index Number)				Combinations Not Allowed (Pin Index Number)			
True Differential		Single-Ended		True Differential		Single-Ended	
Bank	Pin Pair	Bank	Pin	Bank	Pin Pair	Bank	Pin
3A	88 and 89	3B	2	2A	88 and 89	2B	2
	94 and 95		7		94 and 95		7
3B	2 and 3	3A	88	2B	2 and 3	2A	88
	6 and 7		95		6 and 7		95

Figure 3-3 USB Blaster III shown in PC Device Manager

3.5 HPS I/O Pin Assignments

To ensure that the carrier board's HPS pin assignments comply with Altera Agilex 5 specifications, users must adhere to the rules defined in the official pin information documentation. Specifically, HPS peripheral interface pin assignments must be arranged according to the "**Hard Processor System Pin Information for Agilex 5 Devices**" Excel spreadsheet.

Reference Document: Please download the pin information spreadsheet from the following link:

[Hard Processor System Pin Information for Agilex 5 Devices](#) .

Important Notes:

- **Fixed SD/eMMC Pins:** Pins `HPS_IOB_1~3` and `HPS_IOB_5~7` (6 pins in total) are physically dedicated to the HPS SD Card/eMMC interface. When configuring the HPS Pin Mux, users **must** assign these specific pins to the SD/eMMC interface function.
- **Clock Requirement:** A free-running 25 MHz clock must be provided to one of the HPS I/O pins.
- **Compilation Check:** After pin assignment, a full Quartus compilation is required to verify that the HPS I/O pin assignments differ from any conflicts and compile successfully.
- **Series resistors:** To minimize signal reflections and maintain signal integrity, series resistors with values of 20–30 ohms shall be placed on the high-speed signal traces of the USB (60

MHz) and Ethernet RGMII (125 MHz) interfaces. Refer to the Comet A65 Carrier schematic for reference implementation.

3.6 Reset Signals

The system reset architecture relies on the interaction between the Carrier Board and the System MAX10 FPGA on the SOM. The reset propagation flow is described below:

- **HPS_COLD_RESET_n:** This signal serves as the primary HPS cold reset input, routed from the carrier board to the System MAX10 on the SOM. When the carrier board asserts **HPS_COLD_RESET_n**, the System MAX10 detects this event and triggers the internal system reset sequence.
- **SYS_HPS_RST_N:** Generated by the System MAX10, this signal is the active reset source for the HPS logic. Upon the assertion of **HPS_COLD_RESET_n**, the MAX10 drives **SYS_HPS_RST_N** low to reset the HPS. Additionally, this signal is distributed to reset associated HPS peripherals, including the Ethernet PHY, eMMC storage, and UART interfaces.

3.7 Boot Configuration Signals

- **IMAGE_FACTORY** This signal acts as the boot image selector, enabling dual-boot functionality for the SOM. It determines whether the system boots from the factory default image or a user-defined image.
 - ◆ **Factory Boot (Default):** When **IMAGE_FACTORY** is driven High or left Floating, the system is configured to boot from the Factory image.
 - ◆ **User Boot:** When **IMAGE_FACTORY** is driven Low, the system is configured to boot from the User image.

Note: For applications that do not require dynamic dual-boot switching, this signal should be tied High or left floating to ensure the system defaults to the Factory boot configuration.

3.8 Trace-length Matching between SOM and Carrier Boards

If the user needs to perform trace-length matching between SOM and carrier board to maintain differential-pair integrity and high-speed signal quality, they can refer to the “Comet-A65-SOM_B0_IOSkew_20251104.xlsx” spreadsheet which provides the trace lengths and delay times for all signals on the Comet A65 SOM that connect to the B2B connectors.

Mechanical and Heatsink Design

4.1 Introduction

This document details the Comet A65 SOM's mechanical and thermal specifications, featuring an active aluminum heatsink with a 12V, 6000 RPM smart fan.

4.2 Heatsink

The Comet A65 SOM comes equipped with an active aluminum heatsink that efficiently channels heat from the primary heat sources on the module to its large finned surface area for effective dissipation. The active heatsink is equipped with a 12V DC, 60×10 mm, 6000 RPM fan, combined with fan speed control code on the system MAX10. It can automatically adjust the fan speed based on the user's utilization of the SOM FPGA resources.

4.3 Mechanical Dimensions

The table below summarizes the mechanical specifications. Detailed dimensions are provided in the subsequent mechanical drawing.

Table 1-1 Comet A65 SOM Mechanical Specifications

Parameter	Specification
Length of SOM	75 mm
Width of SOM	70 mm
Height of SOM (with heatsink)	30.61 mm

- Mechanical Specifications of Comet A65 SOM without Heatsink (All dimensions in mm)

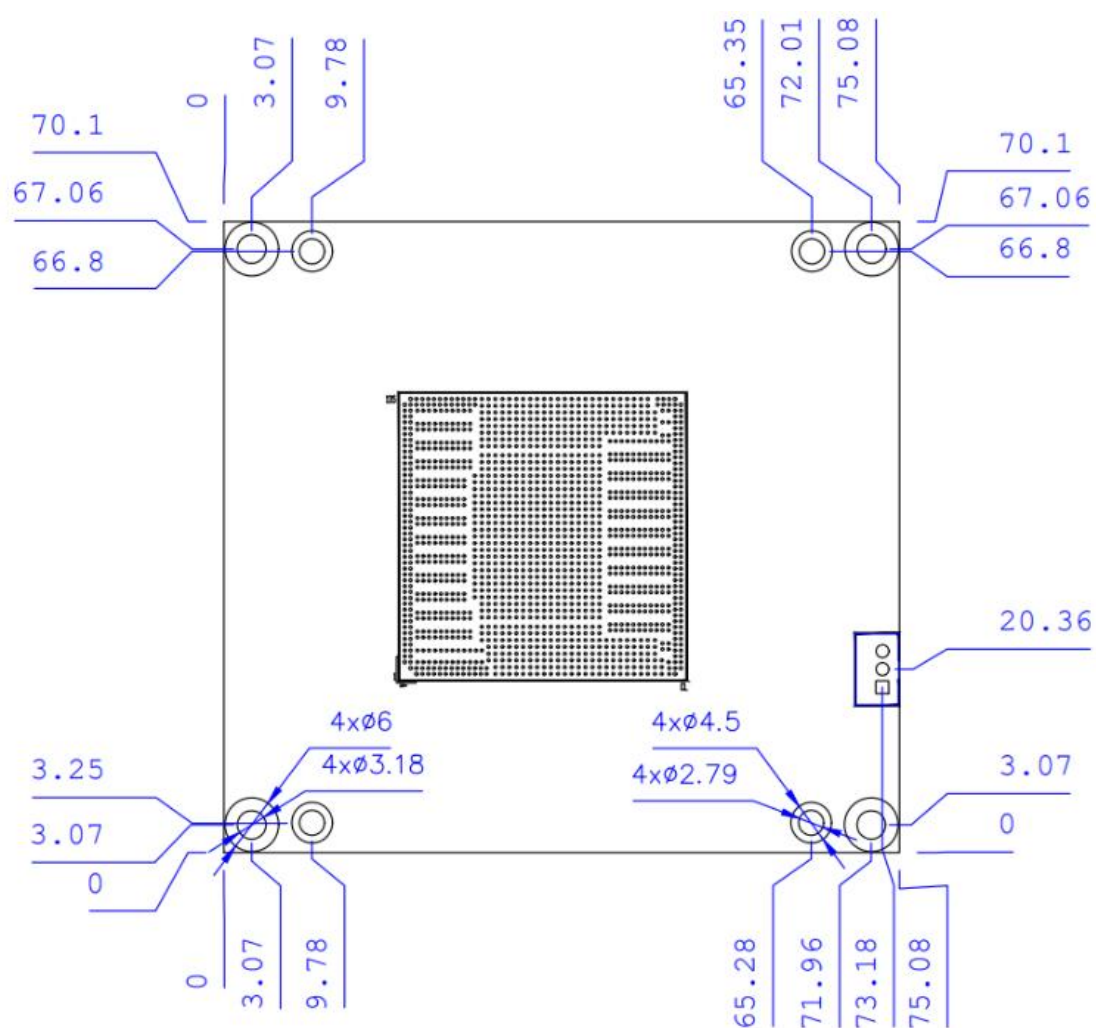


Figure 4-1 Top View

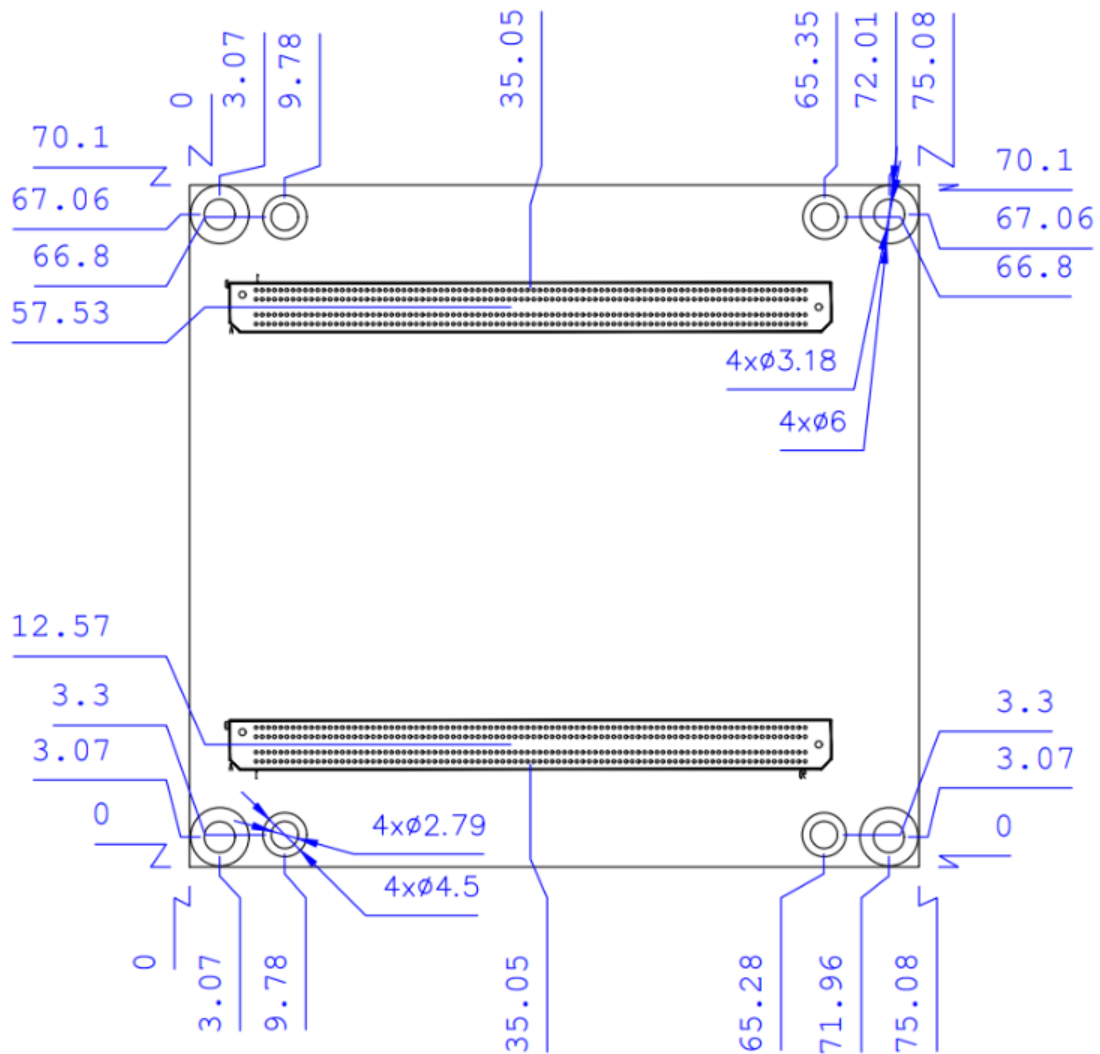


Figure 4-2 Bottom View

- Mechanical Specifications of Comet A65 SOM with Heatsink (All dimensions in mm)

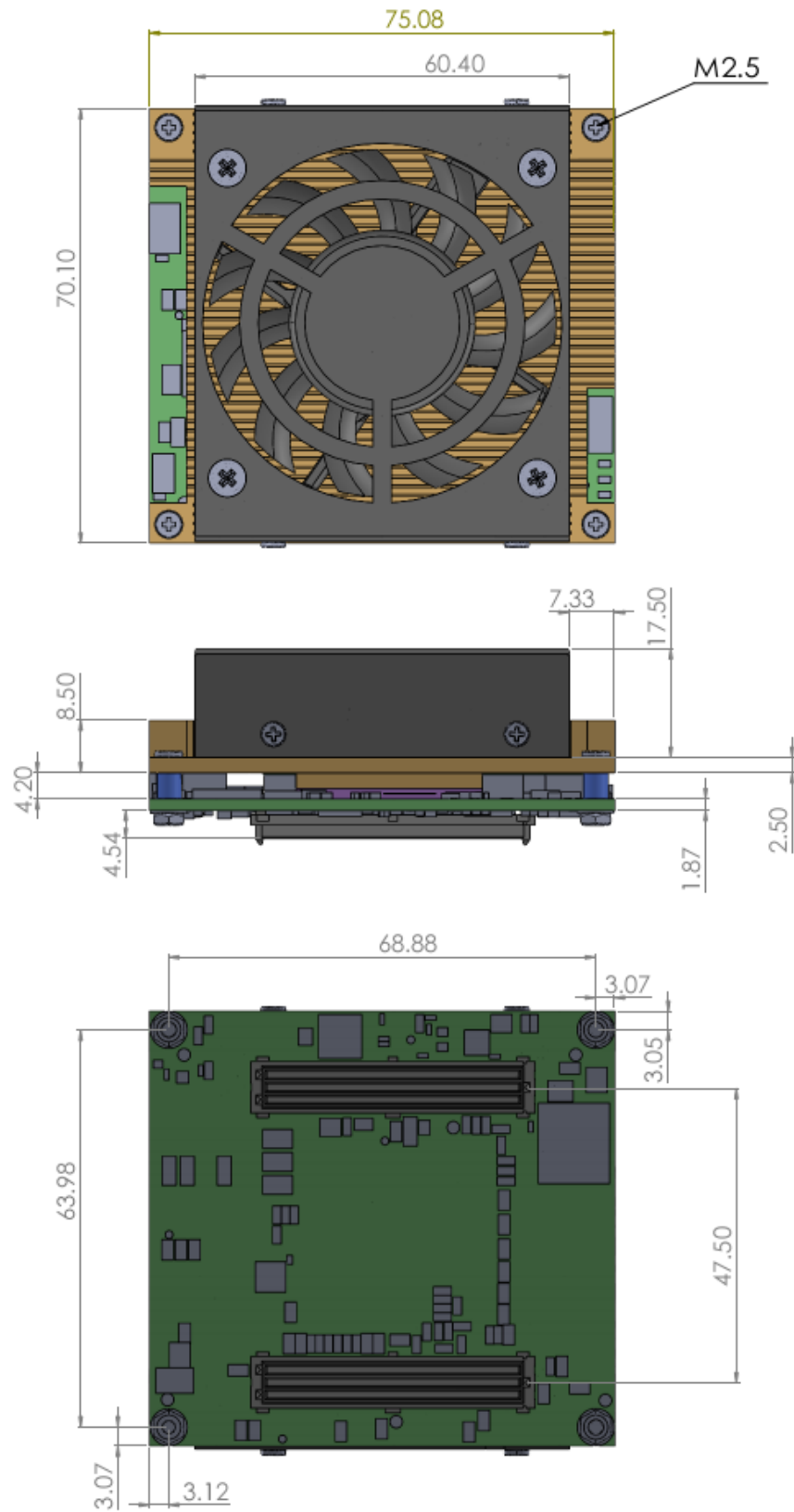


Figure 4-3 Mechanical Specifications of Comet A65 SOM with Heatsink

- The dimensions and details of the Comet A65 stand-offs

The following figures shows how the Comet A65 SOM and heat spreader may be attached to the carrier board using threaded stand-offs.

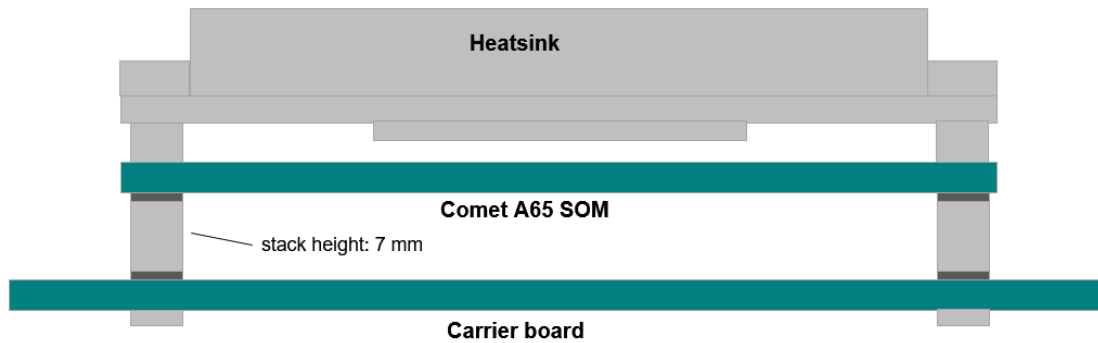


Figure 4-4 Mechanical Stack-up of Comet A65 SOM and Heatsink

The following figures shows the dimensions and details of Comet A65 threaded stand-offs.



Figure 4-5 Detailed Assembly Diagram of Comet A65 SOM Stand-offs

Chapter 5

Assembly & Disassembly

5.1 Assembly & Disassembly for SOM and Carrier

All the screws, washers, and standoffs required to assemble Comet A65 SOM and Carrier together will be pre-installed on the Comet A65 SOM. Here is an assembly and disassembly demonstration video of the SOM and Carrier for customer reference: <https://youtu.be/QWGIqtni40I>

5.2 3D CAD Files

3D CAD models of the Comet A65 SOM are available for carrier board designers.

https://dl2.terasic.com/resources/cometa65/Comet_A65_revB_heatsink_3D_stp.zip

These files can be used to:

- Validate cooling solutions and heatsink designs.
- Check for system-level assembly interferences.
- Ensure proper alignment with B2B connectors.

Power Consumption Measurement

6.1 Power Monitoring System

The Comet A65 SOM features a dedicated power monitor chip equipped with a current sense resistor to measure real-time power consumption. The on-board MAX 10 system controller retrieves this data via the I2C bus and transmits it through the UART interface to the B2B connector. This architecture allows users to access power consumption metrics directly from their carrier board.

Additional Information

Contact Terasic

Users can refer to the following table for technical support and more information of Terasic and our product:

Contact Method	Address
Email	support@terasic.com/sales@terasic.com
Tel	+886-3-575-0880
Website	www.terasic.com
Address	No.80, Fenggong Rd., Hukou Township, Hsinchu County, 303035 Taiwan

Revision History

Date	Version	Changes
2025.12	V1.0	First Version